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EXAMINER	
FEARS, T	
ART UNIT	**PAPER NUMBER**
2511	5

25M1/0605

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DATE MAILED: 06/05/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 20-25 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☒ Claims 20-25 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

The amendment of 21 December 1995 is being entered.

Claim 25 is rejected and prosecution is reopened on claims 20-24 which are considered unpatentable for the reasons set forth below.

A new declaration is required as the "reviewed and understands" clause is missing from the declaration of record.

Claims 20-25 are rejected in view of claims 1-6 of Applicant's patent No. ~~5,093,602~~ 5,448,520 based on non-obviousness/non-statutory type double patenting. DETAILS ARE SET FORTH IN ATTACHMENT "A".

Any inquiry concerning this communication should be directed to Terrell Fears at telephone number (703) 308-0956.

Fears/tj
May 15, 1996

TERRELL W. FEARS
PRIMARY EXAMINER
GROUP 2500

ATTACHED: ATTACHMENT "A"

 Amendment "A"

It should be noted that the present application is a voluntarily filed continuation application not necessitated by restriction. Thus the disclosure supporting claims ~~20-24~~ 20-25 is identical to that of the patent. The claims in both the patent and the application cover the same embodiment disclosed in both the application and the patent [Fig.'s 4A, 4C, and 4E - with the "same precharge circuit" and "sense amplifier"].

A comparison of claims ~~20-24~~ 20-25 in view of claims 1-6 of applicant's Patent No. ~~5,093,602~~ 5,448,520 shows that the patent claims protect the same embodiment as the application claims. Thus the patent claims already provide coverage for the application claims due to the "Comprising" format of the claims. Claim 1 of the patent and claim 20 of the application are compared on page 4. Note that the first two underlined portions of claim 1 of the patent do not appear in application claim 20. These limitations are redundant in that they recite what is already recited in the body of the claim. The amplifier transistors are recited as connected to the data lines and they make-up the amplifier thus the amplifier is **coupled to the data lines**. The sense amplifier defined in the specification amplifies the potential difference between the data lines in Fig.'s 4A, 4C and 4E. The amplifier is a positive feedback differential amplifier. The amplifier recited in claim 20 of the application is a broader recitation than the amplifier clause of the patent. Claim 20 includes the "adapted to amplify a potential difference between the data lines" feature recited in claim 1 of the patent because of the "comprising" language format.

The precharging circuit as disclosed in the patent includes all three recited transistors of claims 20 and 21 of the application. Claim 20 of the application also includes all three transistors even though not specifically recited. The "Comprising" language includes all those elements that make-up the precharging circuit even if not

Page

specifically recited. Thus applicants claim 20 will extend the coverage of claim 1 of the patent. The same reasoning is true for claims ~~21-24~~ 21-25 of the application. Claims 21 recites the second and third transistors of the precharge circuit recited in claim 1 of the patent. Claims ~~22-24~~ 22-25 recite limitations ~~that are also~~ equivalent to those recited in claims 4-6 of the patent.

The recent Policy paper on Double Patenting further explains this situation.

> "There are some unique circumstances where it has been recognized that another type of nonstatutory double patenting is applicable even where the inventions claimed in two or more applications/patents are considered nonobvious over each other. These circumstances are illustrated by the facts before the court in In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968).
>
> Schneller disclosed an invention relating to a wire clip having three elements known in the prior art (A, B, and C), and two features (X and Y) which he had invented that could be used separately or in combination. Schneller acknowledged the best mode of his invention used the two features (X and Y) in combination. The claims of the patent were directed to a wire clip comprising ABCX. Schneller voluntarily filed a divisional application claiming wire clips comprising ABCY and ABCXY. Without determining that the combinations ABCY and ABCXY were obvious over the combination ABCX claimed in the patent, the court affirmed the double patenting rejection. It was observed that the claims in both the patent and the application cover the preferred embodiment disclosed in both the application and the patent (ABCXY). Since patent protection for the metal clips defined by ABCXY, fully disclosed in and covered by the claims of the patent, would be extended by allowance of the appealed claims, the double patenting rejection was affirmed.
>
> In making an analysis for this type of nonstatutory double patenting, the first question is: Is the subject matter recited in the claims of the application fully disclosed in the patent and covered by a claim in the patent? If the answer is no double patenting does not exist. If the answer is yes, the second question is: Whether there is any reason why applicant was prevented from presenting the same claims for examination in the issued patent? If the answer is no, a double patenting rejection is appropriate because, as stated in Schneller:
>
> . even a minimum concern for the public interest requires an applicant to establish that the inventions are in fact independent and distinct and hence that the grant of a patent on the later application will not result in a timewise extension of the protection afforded by his earlier patent. Failing in this, an applicant's remedy lies in filing a terminal disclaimer which will effectively prevent his result.

and further:

> Under the circumstances of the instant case, wherein we find no valid excuse or mitigating circumstances making it either reasonable or equitable to make an exception, and wherein there is no terminal disclaimer, the rule against "double patenting" must be applied.

The claims in both the patent and the application cover the same embodiment disclosed in both the application and the patent [Fig.'s 4A, 4C, and 4E - with the "same precharge circuit" and "sense amplifier"]. Since patent protection for the semiconductor memory defined by claims ~~20-24~~ 20-25 of the application is fully covered by the claims of the patent, said patent protection would be extended by allowance of claims ~~20-24~~ 20-25 of the application and thus a double patenting rejection is necessary.

Using the test for non-statutory double patenting the following findings result.

Is the subject matter recited in the claims of the application fully disclosed in the patent and covered by a claim in the patent? If the answer is no double patenting does not exist. If the answer is yes, the second question is:	YES
Whether there is any reason why applicant was prevented from presenting the same claims for examination in the issued patent?	
If the answer is no, a double patenting rejection is appropriate.	No Reason

The instant application claims covers the subject matter covered by the patent claims and the application claims would unjustifiably extend the right to exclude granted by the patent.

Patent No. 5,448,520	Instant Application
A semiconductor memory comprising:	A semiconductor memory comprising:
a pair of data lines which are formed substantially in parallel to each other;	a pair of data lines which are formed substantially in parallel to each other;
a plurality of word lines, each of which is arranged so as to intersect with both of said data lines of said pair of data lines;	a plurality of word lines, each of which is arranged so as to intersect with both of said pair of data lines;
a plurality of dynamic memory cells, each of which is coupled to one of said word lines and to one of said data lines;	a plurality of dynamic memory cells, each of which is coupled to one of said word lines and to one of said data lines;
an amplifier, coupled to said pair of data lines, adapted to amplify a potential difference between said data lines so as to provide said data lines with a high-level potential and a low-level potential, respectively, wherein said	wherein said amplifier provides said data lines with a high-level potential and a low-level potential, respectively; and
amplifier includes a pair of N-channel MOS transistors and a pair of P-channel MOS transistors, wherein each transistor of said pair of N-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of N-channel MOS transistors, wherein a drain of one of said pair of N-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of N-channel MOS transistors is coupled to the other of said pair of data lines, wherein each transistor of said pair of P-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of P-channel MOS transistors, and wherein a drain of one of said pair of P-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of P-channel MOS transistors is coupled to the other of said pair of data lines; and	an amplifier having a pair of N-channel MOS transistors and a pair of P-channel MOS transistors, wherein each transistor of said pair of N-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of N-channel MOS transistors, wherein a drain of one of said pair of N-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of N-channel MOS transistors is coupled to the other of said pair of data lines, wherein each transistor of said pair of P-channel MOS transistor has a gate cross-coupled to a drain of the other transistor of said pair of P-channel MOS transistors, and wherein a drain of one of said pair of P-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of P-channel MOS transistors is coupled to the other of said pair of data lines,
a *precharging circuit* adapted to set said data lines at a predetermined level when said plurality of dynamic memory cells are in a non-selected state, wherein said predetermined level is an intermediate level between said high-level potential and said low-level potential.	a first switching MOS transistor having a source-drain path provided between said pair of data lines, wherein said first switching MOS transistor sets said pair of data lines at an intermediate level between said high-level potential and said low-level potential when said plurality of memory cells are in a non-selected state.